25-27 and 39-42 will be canceled, claims 19-21 and 28-38 will be amended, and new claims 43-50 will be added upon entry of the present amendment.

Information Disclosure Statements

The applicant submitted an Information Disclosure Statement on August 14, 1998. A Supplemental Information Disclosure Statement was filed on October 28, 1998. The applicant respectfully requests that these Information Disclosure Statements be entered and the documents listed on the attached Forms 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of each of the forms 1449, initialed by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Rejections Under 35 U.S.C.§103

Claims 19-21 and 28-38 are rejected under 35 U.S.C.§103(a) as being unpatentable over Lee (U.S. Patent No. 5,846,859) in view of Aoyama et al. (Aoyama, U.S. Patent No. 4,507,673). The applicant respectfully traverses.

Claim 19 recites a method of using a floating gate transistor having a floating gate electrode and an adjacent amorphous silicon carbide (a-SiC) gate insulator between the floating gate electrode and a substrate comprising, among other limitations, storing data by changing a charge of the floating gate.

Lee is deficient in the following respects. Lee discloses a capacitor in Figure 1 having two SiC layers 24, 28. As the Examiner stated, Lee does not disclose a floating gate transistor, or a method of using a floating gate transistor.

Aoyama does not supply the elements missing in Lee. Aoyama discloses in Figure 2 a FET memory device having a *double gate insulation film construction*. As described in column 2, lines 35-68 of Aoyama, a silicon dioxide (SiO2) gate insulation film 4 is formed over a channel region in a substrate 1 between a source 2 and a drain 3. A silicon carbide (SiC) gate insulation film 5 is formed on the gate insulation film 4. A gate electrode 7 of aluminum is formed on the gate insulation film 5. The memory device is operated to store data in the following manner. Electrons are injected through the SiO2 film 4 and "are mainly trapped in the

interface of the SiO2 film 4 and the SiC film 5 and in the vicinity thereof." Column 2, lines 64-66. Aoyama therefore does not disclose a floating gate transistor, because the structure in Figure 2 has no floating gate. Both the films 4 and 5 are described as insulators. The FET is of "double gate insulation film construction." Column 2, line 37. Furthermore, the SiC film 5 is in direct contact with the gate electrode 7, and so could not hold charge as a floating gate. The applicant respectfully submits that Aoyama also does not disclose a floating gate transistor, or a method of using a floating gate transistor.

Furthermore, there is no suggestion in either Lee or Aoyama for the combination put forward by the Examiner. Lee discloses a capacitor, and Aoyama discloses a FET. The only similarities between the two disclosures are that both are used in memory devices and both have some SiC in their construction.

The applicant respectfully submits that neither Lee or Aoyama, alone or in combination, disclose or suggest a method of using a floating gate transistor having a floating gate electrode and an adjacent amorphous silicon carbide (a-SiC) gate insulator between the floating gate electrode and a substrate comprising, among other limitations, storing data by changing a charge of the floating gate.

Claim 28 recites a method of using a floating gate transistor comprising, among other limitations, programming a floating gate electrode of the floating gate transistor by placing a charge on the floating gate electrode, wherein the floating gate transistor has a barrier energy between the floating gate electrode and a silicon carbide (SiC) gate insulator separating the floating gate electrode from a substrate. For the reasons mentioned above with respect to claim 19, the applicant respectfully submits that neither Lee or Aoyama, alone or in combination, disclose or suggest a method including all the limitations recited in claim 28, or the limitations recited in claims 29-33 that are dependent on claim 28.

Claim 34 recites a method for operating a floating gate transistor comprising, among other limitations, storing data on a floating gate electrode in the floating gate transistor by providing a control voltage on the control line and a write voltage on the data line such that charge is carried from a substrate to the floating gate electrode through a silicon carbide (SiC) gate insulator. For the reasons mentioned above with respect to claim 19, the applicant respectfully submits that neither Lee or Aoyama, alone or in combination, disclose or suggest a

method including all the limitations recited in claim 34, or the limitations recited in claims 35-38 that are dependent on claim 34.

New Claims

The applicant has added new claims 43-50, and respectfully submits that all of the new claims 43-50 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

Respectfully submitted,
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on May 14, 1999.

CANDY BUENDING
Name

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Signature

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